

What is claimed is:

1. A voltage level shifting circuit comprising:
 - a first power supply node supplied with a first power supply potential
 - 5 level;
 - a second power supply node supplied with a second power supply potential level higher than the first power supply potential level;
 - a third power supply node supplied with a third power supply potential level higher than the second power supply potential level;
 - 10 a signal input circuit which is coupled between the first power supply node and the second power supply node, which receives a signal having the first and second power supply potential levels, and which outputs a complementary signal having the first and second power supply potential levels;
 - a complimentary signal input circuit which is coupled to the first power
 - 15 supply node and which includes a first pair of MOS transistors, each of the first MOS transistors has a first withstand voltage and has a first electrode coupled to the first power supply node, a second electrode, and a gate electrode receiving the complementary signal;
 - a load circuit which is coupled to the third power supply node and which
 - 20 includes a second pair of MOS transistors, each of the second MOS transistors has a second withstand voltage higher than the first withstand voltage and has a first electrode coupled to the third power supply node, a second electrode, and a gate electrode;
 - a first voltage down-converting circuit which is coupled between the load
 - 25 circuit and the complimentary signal input circuit and which prevents a potential level exceeding the first withstand voltage from supplying to the complimentary signal input circuit;

a third MOS transistor which is coupled between the third power supply node and an output node, which has the second withstand voltage, and which electrically connects the third power supply node to the output node in response to a voltage potential outputted from the load circuit;

5 a fourth MOS transistor which is coupled between the first power supply node and the output node, which has the first withstand voltage, and which electrically connects the first power supply node to the output node in response to one of the voltage potentials of the complimentary signal; and

10 a second voltage down-converting circuit which is coupled between the third MOS transistor and the fourth MOS transistor and which prevents a potential level exceeding the first withstand voltage from supplying to the fourth MOS transistor.

2. The voltage level shifting circuit according to Claim 1, wherein the
15 first voltage down-converting circuit comprises a fifth pair of MOS transistors, each of which has a first electrode coupled to the load circuit, a second electrode coupled to the corresponding second electrodes of the first MOS transistors, and a gate electrode supplied with a fixed voltage potential level.

20 3. The voltage level shifting circuit according to Claim 2, wherein the fixed voltage potential level is the second power supply potential level.

4. The voltage level shifting circuit according to Claim 1, wherein the
25 second voltage down-converting circuit comprises a sixth MOS transistor which has a first electrode coupled to the third MOS transistor, a second electrode coupled to the fourth MOS transistor, and a gate electrode supplied with a fixed voltage potential level.

5. The voltage level shifting circuit according to Claim 4, wherein the fixed voltage potential level is the second power supply potential level.
- 5 6. The voltage level shifting circuit according to Claim 1, wherein the second pair of MOS transistors constitute a current mirror type load.
7. The voltage level shifting circuit according to Claim 1, further comprising a constant current element which is coupled between the first electrodes of the first MOS transistors and the first power supply node.
- 10 8. The voltage level shifting circuit according to Claim 7, wherein the constant current element comprises a MOS transistor.
- 15 9. A voltage level shift circuit comprising:
a first power supply node supplied with a first power supply potential level;
a second power supply node supplied with a second power supply potential level higher than the first power supply potential level;
20 a third power supply node supplied with a third power supply potential level higher than the second power supply potential level;
a signal input circuit which is coupled between the first power supply node and the second power supply node, which receives a signal having the first and second power supply potential levels, and which outputs a complementary
25 signal having the first and second power supply potential levels;
a complimentary signal input circuit which is coupled to the first power supply node and which includes a first pair of MOS transistors, each of the first

MOS transistors has a first withstand voltage and has a first electrode coupled to the first power supply node, a second electrode, and a gate electrode receiving the complementary signal;

5 a load circuit which is coupled to the third power supply node and which includes a second pair of MOS transistors, each of the second MOS transistors has a second withstand voltage higher than the first withstand voltage and has a first electrode coupled to the third power supply node, a second electrode, and a gate electrode;

10 a first voltage descending circuit which is coupled between the load circuit and the complimentary signal input circuit and which prevents a potential level exceeding the first withstand voltage from supplying to the complimentary signal input circuit;

15 a third MOS transistor which is coupled between the third power supply node and an output node, which has the second withstand voltage, and which electrically connects the third power supply node to the output node in response to a voltage potential outputted from the load circuit;

20 a fourth MOS transistor which is coupled between the first power supply node and the output node, which has the first withstand voltage, and which electrically connects the first power supply node to the output node in response to one of the voltage potentials of the complimentary signal; and

a second voltage descending circuit which is coupled between the third MOS transistor and the fourth MOS transistor and which prevents a potential level exceeding the first withstand voltage from supplying to the fourth MOS transistor.

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10. The voltage level shifting circuit according to Claim 9, wherein the first voltage descending circuit comprises a fifth pair of MOS transistors, each of

which has a first electrode coupled to the load circuit, a second electrode coupled to the corresponding second electrodes of the first MOS transistors, and a gate electrode supplied with a fixed voltage potential level.

5 11. The voltage level shift circuit according to Claim 10, wherein the fixed voltage potential level is the second power supply potential level.

12. The voltage level shift circuit according to Claim 9, wherein the second voltage down-converting circuit comprises a sixth MOS transistor which
10 has a first electrode coupled to the third MOS transistor, a second electrode coupled to the fourth MOS transistor, and a gate electrode supplied with a fixed voltage potential level.

13. The voltage level shift circuit according to Claim 12, wherein the
15 fixed voltage potential level is the second power supply potential level.

14. The voltage level shift circuit according to Claim 9, wherein the second pair of MOS transistors constitute a current mirror type load.

20 15. The voltage level shift circuit according to Claim 9, further comprising a constant current element which is coupled between the first electrodes of the first MOS transistors and the first power supply node.

16. The voltage level shift circuit according to Claim 15, wherein the
25 constant current element comprises a MOS transistor.